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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
ODOM, CURTIS B	

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

SK

Office Action Summary	Application No.	Applicant(s)	
	10/039,794	SON ET AL.	
	Examiner	Art Unit	
	Curtis B. Odom	2611	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (previously cited in Office Action 11/29/2005) in view of Cho (previously cite in Office Action 5/11/2006) and in further view of Ko (previously cited in Office Action 11/29/2005).

Regarding claim 1, Tanaka et al. discloses a method of recording digital data, comprising the steps of:

binding (column 12, lines 22-39) input digital data into 2D data (unit) blocks comprising a plurality of bytes; and

8/15 conversion (column 12, lines 65-column 13, line 30) for modulation-coding each byte of the unit blocks according a code conversion table (see Figs. 2 and 3).

Tanaka et al. discloses the modulation-coded data contains a merging bit separating the data blocks (column 9, lines 9-17) but does not specifically disclose adding at least one merging bit followed by the modulation-coded unit block and recording byte-unit information indicating the number of bytes comprising each unit block together with each modulation-coded block to which the at least one merging bit was added.

However, Cho discloses EFM modulation-coding bytes (8 bits) of data (column 7, lines 3-16). Cho also discloses selecting at least one merging bit and combining the merging bit with each modulated symbol (column 7, lines 27-29). Cho further discloses the merging bit is followed by the 14 bit symbols in column 5, lines 53-67. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the method of Tanaka et al. with the teachings of Cho since Cho states that selecting the correct merging bit minimizes the direct current component of reproduced signals (column 2, lines 25-39).

Ko further discloses EFM modulation-coding bytes (8 bits) of data (see column 4, lines 7-30) including using a merging bit with the coding. Ko further discloses encoding (recording) byte unit information using identifying bits (see column 4, lines 25-30) which indicate the runlength (number of bits) converted (modulated) in the modulated-coded block to which the merging bit was added (see column 9, lines 59-57). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the coding of Tanaka et al.

and Cho with the identifying bits of Ko since Ko states to increase the efficiency of the EFM code (see column 10, lines 23-27).

Regarding claim 2, which inherits the limitations of claim 1, Tanaka et al. discloses each data block comprises a plurality of bytes (column 12, lines 27-39), but Tanaka et al. and Cho do not specifically disclose each block comprises three to seven bytes. However, Tanaka et al. further discloses the data is written to an optical disk in blocks of 168x168 bytes. Threrefore, it would have been obvious to one skilled in the art at the time the invention was made that since data could be written in blocks of 168x168 bytes that data could have also been written to the optical disk in blocks of 3 to 7 bytes.

Regarding claim 3, Cho further discloses adding three merging bits (column 7, lines 11-16). It would have been obvious to one skilled in the art to include this feature since Cho states that selecting the correct merging bit minimizes the direct current component of reproduced signals (column 2, lines 25-39)

Regarding claim 4, Tanaka et al. discloses each of the plurality of bytes is modulation-coded (converted) into a code word of a fifteen bit length by an 8/15 conversion table (column 13, lines 11-30).

Regarding claim 5, Cho further discloses adding the at least one merging bit comprises comparing (column 7, lines 30-35) a digital sum value (wherein the digital sum (DSV) value represents an RDS) of a present symbol formed by a present merge bit to a DSV of a previous symbol formed by a previous merge bit such that the DSV is minimized to "0" (see also column 2, lines 26-39) without violating 3T or 11T RLL constraints. It would have been obvious to one

skilled in the art to include this feature since Cho states that selecting the correct merging bit minimizes the direct current component of reproduced signals (column 2, lines 25-39).

Regarding claim 6, Cho further discloses primarily generating (outputting) at least one merging bit (column 7, lines 11-16) followed by combination (column 7, lines 26-29) of the merging bit and the symbol to produce the modulation-coded present symbol, while simultaneously replacing (updating) the DSV (column 7, lines 30-35, wherein the DSV represents the RDS) up to the present unit block minimize the DSV value for addition of at least one merging bit for a next symbol. It would have been obvious to one skilled in the art to include this feature since Cho states that selecting the correct merging bit minimizes the direct current component of reproduced signals (column 2, lines 25-39).

Regarding claim 7, Tanaka et al. discloses a method of recording digital data, comprising the steps of:

performing (column 12, line 65-column 13, line 30) 8/15 conversion (modulation-coding) to an input data block in the unit of m byte and simultaneously producing a DSV of the input data block (Fig. 8, block 807, column 17, lines 33-56, wherein DSV represents an RDS).

Tanaka et al. does not specifically disclose evaluating the RDS of the input data block and an RDS of the previous block to select a merging bit;

outputting the selected at least one merging bit, following by modulation-coded input data block, and updating the RDS for selecting at least one merging bit for a next input data block (column 22, lines 3-25); and

recording byte-unit information indicating the number of bytes comprising the input data block together with each modulation-coded block and the selected at least one merging bit.

However, Cho discloses adding the at least one merging bit comprises comparing (column 7, lines 30-35) a digital sum value (wherein the digital sum (DSV) value represents an RDS) of a present symbol formed by a present merge bit to a DSV of a previous symbol formed by a previous merge bit such that the DSV is minimized to "0" (see also column 2, lines 26-39) without violating 3T or 11T RLL constraints. Cho further discloses primarily generating (outputting) at least one merging bit (column 7, lines 11-16) followed by combination (column 7, lines 26-29) of the merging bit and the symbol to produce the modulation-coded present symbol, while simultaneously replacing (updating) the DSV (column 7, lines 30-35, wherein the DSV represents the RDS) up to the present unit block minimize the DSV value for addition of at least one merging bit for a next symbol. Cho further discloses the merging bit is followed by the 14 bit symbols in column 5, lines 53-67. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the method of Tanaka et al. with the teachings of Cho since Cho states that selecting the correct merging bit minimizes the direct current component of reproduced signals (column 2, lines 25-39).

Ko further discloses EFM modulation-coding bytes (8 bits) of data (see column 4, lines 7-30) including using a merging bit with the coding. Ko further discloses encoding (recording) byte unit information using identifying bits (see column 4, lines 25-30) which indicate the runlength (number of bits) converted (modulated) in the modulated-coded block to which the merging bit was added (see column 9, lines 59-57). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the coding of Tanaka et al.

and Cho with the identifying bits of Ko since Ko states to increase the efficiency of the EFM code (see column 10, lines 23-27).

Regarding claim 8, Tanaka et al. discloses a method of converting digital data, comprising the steps of:

binding (column 12, lines 22-39) input digital data into 2D data (unit) blocks comprising a plurality of bytes; each block also including a merging bit (column 13, lines 9-17).

Tanaka et al. does not specifically disclose adding at least one merging bit followed by the modulation-coded unit block and recording byte-unit information indicating the number of bytes comprising the input data block together with each modulation-coded block and the selected at least one merging bit, and further decoding each unit block using the corresponding byte-unit information.

However, Cho discloses EFM modulation-coding bytes (8 bits) of data (column 7, lines 3-16. Cho also discloses selecting at least one merging bit and combining the merging bit with each modulated symbol (column 7, lines 27-29). Cho further discloses the merging bit is followed by the 14 bit symbols in column 5, lines 53-67. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the method of Tanaka et al. with the teachings of Cho since Cho states that selecting the correct merging bit minimizes the direct current component of reproduced signals (column 2, lines 25-39).

Ko further discloses EFM modulation-coding bytes (8 bits) of data (see column 4, lines 7-30) including using a merging bit with the coding. Ko further discloses encoding (recording) byte unit information using identifying bits (see column 4, lines 25-30) which indicate the

runlength (number of bits) converted (modulated) in the modulated-coded block to which the merging bit was added (see column 9, lines 59-57). The identifying bits are then used to decode EFM modulated block data (see column 10, lines 1-22). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the coding of Tanaka et al. and Cho with the identifying bits of Ko since Ko states to increase the efficiency of the EFM code (see column 10, lines 23-27).

Regarding claim 9, which inherits the limitations of claim 8, Tanaka et al. discloses each data block comprises a plurality of bytes (column 12, lines 27-39), but Tanaka et al. and Cho do not specifically disclose each block comprises three to seven bytes. However, Tanaka et al. further discloses the data is written to an optical disk in blocks of 168x168 bytes. Threrefore, it would have been obvious to one skilled in the art at the time the invention was made that since data could be written in blocks of 168x168 bytes that data could have also been written to the optical disk in blocks of 3 to 7 bytes.

Regarding claim 10, Cho further discloses the at least one merging bit is added such that a DSV value (wherein a DSV represents a RDS) is minimized to "0" without violating 3T and 11T RLL constraints (column 2, lines 25-39 and column 7, lines 30-35).

Regarding claim 11, Tanaka et al. discloses binding (column 12, lines 22-39) input digital data into 2D data (unit) blocks comprising a plurality of bytes; and

8/15 conversion (column 12, lines 65-column 13, line 30) for modulation-coding each byte of the unit blocks according a code conversion table (see Figs. 2 and 3).

Tanaka et al. does not disclose comparing a RDS of a present input data block to a RDS of the previous data block to allocate the merging bit for the present data block so that the RDS is minimized without violating RLL restraints;

primarily outputting at least one merging bit, followed by the modulation coded present data block, while simultaneously updating the RDS up to the present block to prepare for allocation of at least one merging bit for a next block; and

recording byte-unit information indicating the number of bytes comprising each unit block together with each modulation-coded present block and the at least one merging bit.

However, Cho discloses adding the at least one merging bit comprises comparing (column 7, lines 30-35) a digital sum value (wherein the digital sum (DSV) value represents an RDS) of a present symbol formed by a present merge bit to a DSV of a previous symbol formed by a previous merge bit such that the DSV is minimized to "0" (see also column 2, lines 26-39) without violating 3T or 11T RLL constraints. Cho further discloses primarily generating (outputting) at least one merging bit (column 7, lines 11-16) followed by combination (column 7, lines 26-29) of the merging bit and the symbol to produce the modulation-coded present symbol, while simultaneously replacing (updating) the DSV (column 7, lines 30-35, wherein the DSV represents the RDS) up to the present unit block minimize the DSV value for addition of at least one merging bit for a next symbol. Cho further discloses the merging bit is followed by the 14 bit symbols in column 5, lines 53-67. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the method of Tanaka et al. with the teachings

of Cho since Cho states that selecting the correct merging bit minimizes the direct current component of reproduced signals (column 2, lines 25-39).

Ko further discloses EFM modulation-coding bytes (8 bits) of data (see column 4, lines 7-30) including using a merging bit with the coding. Ko further discloses encoding (recording) byte unit information using identifying bits (see column 4, lines 25-30) which indicate the runlength (number of bits) converted (modulated) in the modulated-coded block to which the merging bit was added (see column 9, lines 59-57). The identifying bits are then used to decode EFM modulated block data (see column 10, lines 1-22). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the coding of Tanaka et al. and Cho with the identifying bits of Ko since Ko states to increase the efficiency of the EFM code (see column 10, lines 23-27).

Regarding claim 12, the claim includes similar limitations to the above rejection of claim 2, which is applicable hereto.

Regarding claim 13, the claim includes similar limitations to the above rejection of claim 3, which is applicable hereto.

Regarding claim 14, the claim includes similar limitations to the above rejection of claim 4, which is applicable hereto.

Regarding claim 15, the claim includes similar limitations to the above rejection of claim 2, which is applicable hereto.

Regarding claim 16, the claim includes similar limitations to the above rejection of claim 3, which is applicable hereto.

Regarding claim 17, the claim includes similar limitations to the above rejection of claim 3, which is applicable hereto.

Regarding claim 18, the claim includes similar limitations to the above rejection of claim 4, which is applicable hereto.

Regarding claim 19, the claim includes similar limitations to the above rejection of claim 5, which is applicable hereto.

Regarding claim 20, the claim includes similar limitations to the above rejection of claim 6, which is applicable hereto.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Curtis B. Odom whose telephone number is 571-272-3046. The examiner can normally be reached on Monday- Friday, 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Curtis Odom
June 11, 2007